

## WE CLAIM:

1. A device, comprising:
  - 5 a processor card;
  - a first memory device mounted upon said processor card, said first memory device including a first address pin and a second address pin; and
  - a second memory device mounted upon said processor card, said second memory device including a third address pin and a fourth address pin,
  - 10 said first address pin and said third address pin being functionally equivalent address pins, said second address pin and said fourth address pin being functionally equivalent address pins,
  - wherein said first address pin and said fourth address pin are electrically coupled to thereby concurrently receive a first address bit signal, and
  - 15 wherein said second address pin and said third address pin are electrically coupled to thereby concurrently receive a second address bit signal.
2. The device of claim 1, wherein
  - said first memory device is mounted to a front side of said
  - 20 processor card; and
  - said second memory device is mounted to a rear side of said processor card.
3. The device of claim 2, wherein
  - 25 said first address pin and said fourth address pin are aligned; and
  - said second address pin and said third address pin are aligned.

4. The device of claim 1, wherein  
said first memory device is a static random access memory; and  
said second memory device is a static random access memory.

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5. The device of claim 1, wherein  
said first memory device further includes a fifth address pin; and  
said second memory device further includes a sixth address pin,  
said fifth address pin and said sixth address pin being electrically coupled to  
10 thereby concurrently receive a third address bit signal.

6. The device of claim 5, wherein  
said fifth address pin and said sixth address pin are functionally  
dissimilar address pins.

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7. The device of claim 5, wherein  
said first memory device further includes a seventh address pin;  
and  
said second memory device further includes an eighth address pin,  
20 said seventh address pin and said eighth address pins being electrically coupled  
to thereby concurrently receive a fourth address bit signal.

8. The device of claim 7, wherein  
said fifth address pin and said eighth address pin are functionally  
equivalent address pins; and  
5 said sixth address pin and said seventh address pin are functionally  
equivalent address pins.
9. A system, comprising:  
a first memory device including a first address pin and a second  
10 address pin;  
a second memory device including a third address pin and a fourth  
address pin, said first address pin and said third address pin being functionally  
equivalent address pins, said second address pin and said fourth address pin  
being functionally equivalent address pins; and  
15 a microprocessor operable to concurrently provide a first address  
bit signal to said first address pin and said fourth address pin, said  
microprocessor further operable to concurrently provide a second address bit  
signal to said second address pin and said third address pin.
- 20 10. The system of claim 9, further comprising:  
a processor card having said first memory device and said second  
memory device mounted thereon.

11. The system of claim 10, wherein  
said first memory device is mounted to a front side of said  
processor card; and

5               said second memory device is mounted to a rear side of said  
processor card.

12. The system of claim 11, wherein  
said first address pin and said fourth address pin are aligned; and  
10               said second address pin and said third address pin are aligned.

13. The system of claim 9, wherein  
said first memory device is a static random access memory; and  
said second memory device is a static random access memory.

15               14. The system of claim 9, wherein  
said first memory device further includes a fifth address pin;  
said second memory device further includes a sixth address pin;

and  
20               said microprocessor is further operable to concurrently provide a  
third address bit signal to said fifth address pin and said sixth address pin.

15. The system of claim 14, wherein  
said fifth address pin and said sixth address pin are functionally  
25       dissimilar address pins.

16. The system of claim 14, wherein  
said first memory device further includes a seventh address pin;  
said second memory device further includes an eighth address; and  
5 said microprocessor is further operable to concurrently provide a  
fourth address bit signal to said seventh address pin and said eighth address pin.

17. The system of claim 16, wherein  
said fifth address pin and said eighth address pin are functionally  
10 equivalent address pins; and  
said sixth address pin and said seventh address pin are functionally  
equivalent address pins.

18. The system of claim 9, wherein  
15 said microprocessor includes a multiplexor operable to provide said  
first address bit signal and said second address bit signal in response to a control  
signal indicative of a cache configuration corresponding to said first address bit  
signal and said second address bit signal.

20 19. The system of claim 14, wherein  
said microprocessor includes a multiplexor operable to provide said  
first address bit signal, said second address bit signal, and said third address bit  
signal in response to a control signal indicative of a cache configuration  
corresponding to said first address bit signal, said second address bit signal, and  
25 said third address bit signal.

20. The system of claim 16, wherein  
said microprocessor includes a multiplexor operable to provide said  
first address bit signal, said second address bit signal, said third address bit  
5 signal, and said fourth address bit signal in response to a control signal indicative  
of a cache configuration corresponding to said first address bit signal, said  
second address bit signal, said third address bit signal, and said fourth address  
bit signal.

10 21. A method, comprising:  
operating a microprocessor to generate a first set of at least two  
address bit signals, said first set of at least two address bit signals being  
indicative of a first cache configuration; and  
operating said microprocessor to generate a second set of at least  
15 two address bit signals, said second set of at least two address bit signals being  
indicative of said second cache configuration of said plurality of cache  
configurations.

22. The method of claim 21, further comprising:  
20 operating a microprocessor to select said first cache configuration  
of a plurality of cache configurations;  
operating said microprocessor to provide a control signal indicative  
of said selection of said first cache configuration; and  
operating said microprocessor to concurrently provide said first set  
25 of at least two address bit signals to a first memory device and a second memory  
device in response to said control signal.

23. A method, comprising:

operating a microprocessor to select a first cache configuration of a plurality of cache configurations; and

5 subsequently operating said microprocessor to concurrently provide a set of at least two address bit signals to a first memory device and a second memory device, said set of at least two address bit signals being representative of said selection of said first cache configuration.

10 24. The method of claim 23, further comprising:

operating a microprocessor to provide a control signal indicative of a said selection of a first cache configuration, said operating of said microprocessor to concurrently provide said set of at least two address bit signals to said first memory device and said second memory device is in response to

15 said control signal.

25. A method, comprising:
- providing a processor board including a first conductor and a second conductor;
- 5 providing a first memory device including a first address pin and a second address pin;
- providing a second memory device including a third address pin and a fourth address pin, said first address pin and said fourth address pin being functionally equivalent address pins, said second address pin and said third
- 10 address pin being functionally equivalent address pin;
- mounting said first memory device on said processor card, said first address pin contacting said first conductor, said second address pin contacting said second conductor;
- mounting a second memory device said processor card, said third
- 15 address pin contacting said first conductor whereby said first address pin and said third address pin are electrically coupled, said fourth address pin contacting said second conductor whereby said second address pin and said fourth address pin are electrically coupled.
- 20 26. The method of claim 25, wherein
- said mounting of said first memory device on said processor card includes mounting first memory device said mounted on a front side of said processor card, and
- said mounting of said second memory device on said processor
- 25 card includes mounting said second memory device said mounted on a rear side of said processor card.



27. The method of claim 26, wherein  
said mounting of said second memory device said on said  
processor card includes aligning said first address pin and said third address pin  
5 and aligning said second address pin and fourth address pin are aligned.